Novel Solid-State Memory Read Mechanism Not Employing Voltage Draining for Enhanced Data Integrity in Support of Increasing MLC Level Counts

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Introduction

Solid-state memory holds the theoretical potential to support capacities of data storage far outstripping commercially available solid-state products which, at best, can reliably employ five distinct levels of charge in each voltage cell. As reading the contents of a voltage cell utilizing conventional methods requires draining part of stored energy of that cell, the process of reading the contents of voltage cells is intrinsically corruptive to the data stored therein. While the restoration of the intended voltage level (once per every 100 read operations, for instance) is instrumental to SSD operation, other factors such as the reliability of voltage meters and the durability of voltage cells limit the number of MLCs that commercially available SSDs can practically employ.

A theoretical design concept based upon the controlled release and re-injection of three electrons into a charged voltage cell and the precision (femtosecond) measurement of the interval between their release measured by advanced, miniaturized atomic timing may eventually make possible MLC counts that exceed 250,000. It may take several years of additional engineering work to finalize the earliest prototypes based upon this approach, primarily due to the need to finalize development of the needed advanced atomic timing mechanisms.

In the interim, SSD technology may be improved by a design not reliant upon draining the voltage of a voltage cell in order to assess its charge level.

Abstract

In order to facilitate the leap from a handful of MLCs to dozens or perhaps hundreds, two primary modifications to existing design are required. In addition to a novel voltage level assessment mechanism not requiring the draining of voltage, voltage gating mechanisms that control the flow of energy into the voltage cells must be modified to make possible the charging of the voltage cells in increasingly minute increments. This mechanism would work hand-in-glove with the novel voltage assessment mechanism in order to allow for voltage cells to be charged with a level of precision that falls short of an electron-count-specific value (something which may eventually be possible utilizing the aforementioned timing-based approach) but which far outstrips present-day commercially available mechanisms.

The precise voltage content of a voltage cell may be accurately assessed by means of the emission of polarity-controlled light as near as possible to the exterior of the voltage cell wherein both the proximity of the light to the voltage

cell and its polarity are controlled with extreme precision. As the voltage contained within an individual cell increases, so does its resident magnetic field. The emission of single wavelength of light with a 45-degree polarity may be used as the basis of a novel voltage metering mechanism as its polarity would be altered to an extent measured in fractions of a degree, with these minute differences in polarity being easily measurable, particularly by gathering data from multiple light emissions and analyzing data from polarity-metric cylindrical semiconductors.

As this metering mechanism requires "magnetic quiet," it would be necessarily to employ anti-ferromagnetic materials in the outer layers of the device to preclude unwanted magnetic flux from external sources.

Measures would need to be taken to prevent interference from internal sources of magnetic flux, the most likely of which would result from the use of conventional modes of conveyance of electricity to voltage cells sc. copper wires. These conventional delivery avenues for current to voltage cells would be undesirable both as they would deliver too much current too quickly (at hundreds of MLCs) and the flow of current would create magnetic fields corruptive to the aforementioned read mechanism.

Two primary measures can be taken to prevent internal interference with a polarity-metric-based voltage cell read mechanism. The first is to employ parallel hydrogen nanowires for delivering current to voltage cells, with greater numbers of these wires being utilized in tandem in order to facilitate faster charging and as few as one wire being utilizing to make fine adjustments to voltage. The second precaution would be to perform read operations only at times when there are no nearby write operations transpiring. These precautions would not significantly impair the performance of the mechanism given that only nanoseconds would be required for full magnetic quiet to be restored after a nearby write operation.

Conclusion

The technology to achieve the goal of building a solid-state memory device not requiring the draining of voltage cells in order to assess their level of charge already exists. This sort of approach can comfortably enable the differentiation of a minimum of 1,200 unique levels of charge, implying an increase in data storage capacity of 240 fold over commercially available designs.

The square footage, energy and financial cost associated with maintaining data centers would be proportionally attrited by the development of this technology, making it a candidate for immediate development.